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Arch reDocket No.: SON-2810
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Reexamination Application of:
Yoshitaka Kayukawa et al.

Application No.: 10/647,217 Confirmation No.: 1901

Filed: August 26, 2003 Art Unit: 2138

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD FOR TESTING SAME Examiner: D. B. Gandhi

AMENDMENT AFTER FINAL ACTION UNDER 37 C.F.R. 1.116

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Office Action dated January 29, 2007, finally rejecting claims 1-23, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 14 of this paper.